



## DESIGN OF MEDIAN FILTER IN QUANTUM-DOT CELLULAR AUTOMATA FOR IMAGE PROCESSING APPLICATIONS

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### Abstract

In this paper, a new layout of the median filter by using Quantum-dot cellular automata (QCA) is designed. This filter is designed using one hot encoding technique. A new algorithm for designing median filter is proposed using majority logic. The 1-bit median finding architecture occupies area of  $0.05 \mu\text{m}^2$ , with a delay of 0.5 clk. The proposed median finding architecture is also extended to higher bit sizes with optimized performance. The uniqueness of our n-bit median finding architecture is that for any bit size the delay for finding the median value is same which is 0.5 clk because every majority gates are working independently. Therefore for faster operation, this majority logic-based technology is highly congruous. All the QCA circuits are implemented in QCA Designer software.

### 1. Introduction

Median filtering is basically used in image processing applications which are basically used for the noise reduction in the image. The pixels of the image are sorted, and the middle position of that sorted value is known as the median. These pixels of the image are replaced by its median value [1]. There are different types of sorting algorithms like quick sort, bubble sort, etc. are

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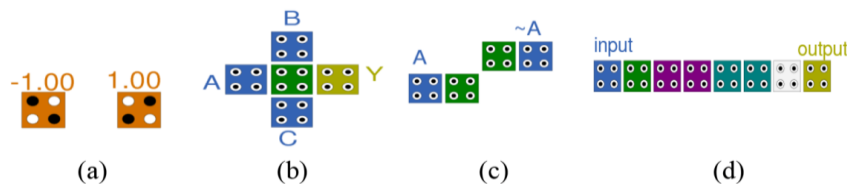
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present. But these sorting algorithms are not very much efficient in designing hardware. Here we proposed a new algorithm using majority logic for finding the median which is very much efficient and fast in operation. The basics of QCA and an algorithm for the median filter using QCA are described in section 2 and section 3 respectively. Finally, the conclusion is presented in section 4.

### 2. QCA Basics

Quantum-dot cellular automata (QCA) is a technique which consists of an array of cells & each cell contains four quantum dots which are arranged in a square pattern. The cell consists of two mobile electrons that can tunnel between the dots [2][3]. Electrons cannot be tunneled out due to the potential barriers between the cells. Here data are moved from one point to another of the cells by transferring its polarization value. In this polarization state ‘-1’ refers to logic ‘0’ and ‘+1’ refers to logic ‘1’. Some universal gates like majority gate & inverter have been made by using QCA [4-8]. If one value among the inputs of the majority gate is given by ‘0’ then it will behave like an AND gate. Similarly, if one value among the inputs of the majority gate is given by ‘1’, then it will behave like an ‘OR’ gate. The QCA inverter can be implemented by different types of cell configuration. The QCA wire can be constructed by connecting the QCA cells back to back. Figure 1a shows QCA cells, Figure 1b shows majority gate, Figure 1c shows inverter and Figure 1c shows binary wire [9-12].



**Figure 1.** QCA basics (a) QCA cell (b) majority gate (c) inverter (d) binary wire.

### 3. Proposed Median Filter Architecture

Here a new architecture for finding the median is proposed. Figure 2 shows the median finding and encoding diagrams. Here, for example, 3×3 size

matrix is considered with nine numbers present. The maximum size of each number is considered as a maximum of 4-bit in size. Here the numbers are in the ascending order as 2, 3, 4, 6, 7, 8, 10, 12, and 15. By using one-hot encoding method, a median filter has been designed. By using this method, the input data can be decoded without using the decoder.

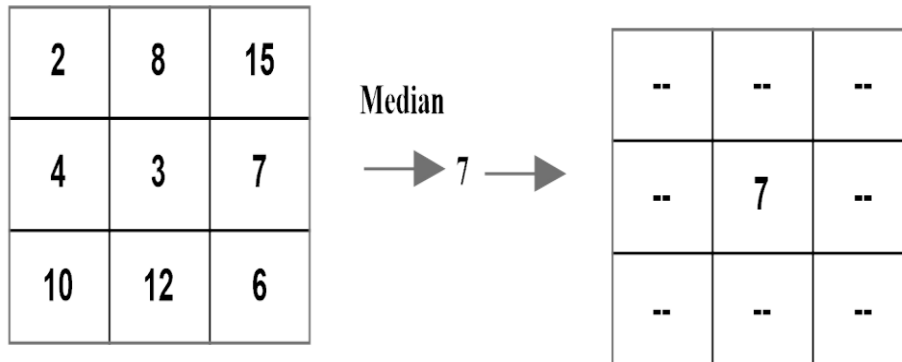


Figure 2. The median finding of a 3x3 matrix.

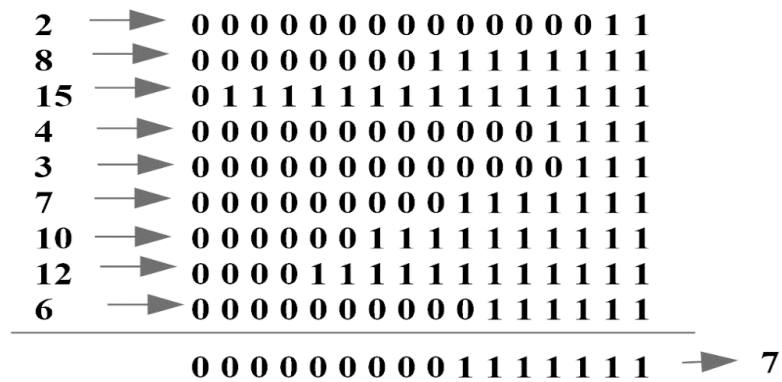
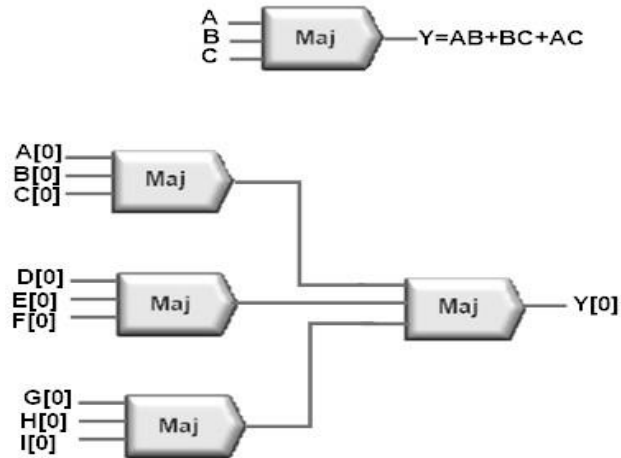
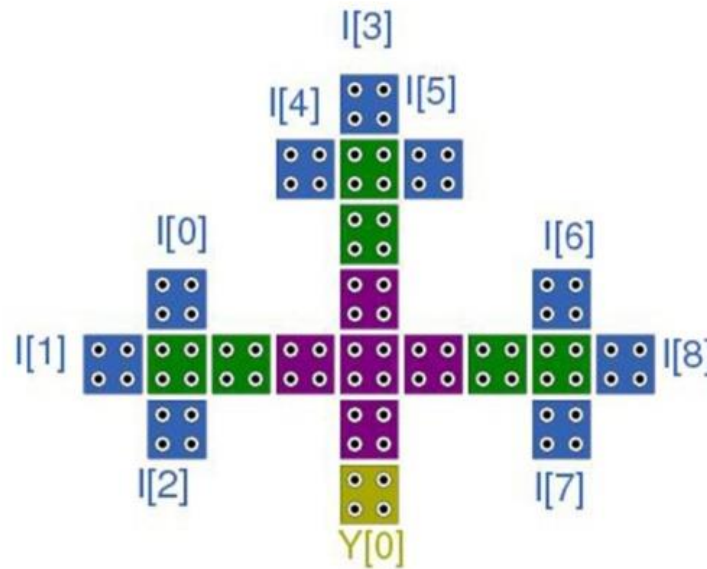


Figure 3. Median finding one hot encoding.



**Figure 4.** Median Filter architecture for each bit using Majority Gates.

Here every number is represented by one hot encoding, for example, 2 digit can be written as “0000000000000011”. Here 16 numbers digits are present in encoded data, for making of all possible combinations of 4-bit size number. Similarly, 8 digits can be represented as “0000000011111111”. Similarly, all the numbers are entered in one hot encoding format. Now in each column, nine numbers of bits are present. In each column, the majority number, i.e., 1 or 0 is selected. The majority value of each column will be the median value of the input nine numbers. This circuit can be suitably designed with majority-logic based circuits such as Quantum-dot cellular automata. Figure 4 shows the majority gates based circuit to find out a lower bit of final median (i.e.,  $Y[0]$  in this case). Figure 5 shows the QCA layout of the median filter architecture for a single column of Figure 4. For this column, four numbers of majority gates are needed. Therefore designing 4-bit numbers median architecture needs 144 (i.e.,  $16 \times 9$ ) numbers of majority gate. The advantage of this architecture is that all columns can find its value independently. Therefore the Median value can be generated, with a clock delay of single column gates. Here  $I[0]$  to  $I[8]$  are input numbers of any single column, and  $Y[0]$  is an output value of that column.

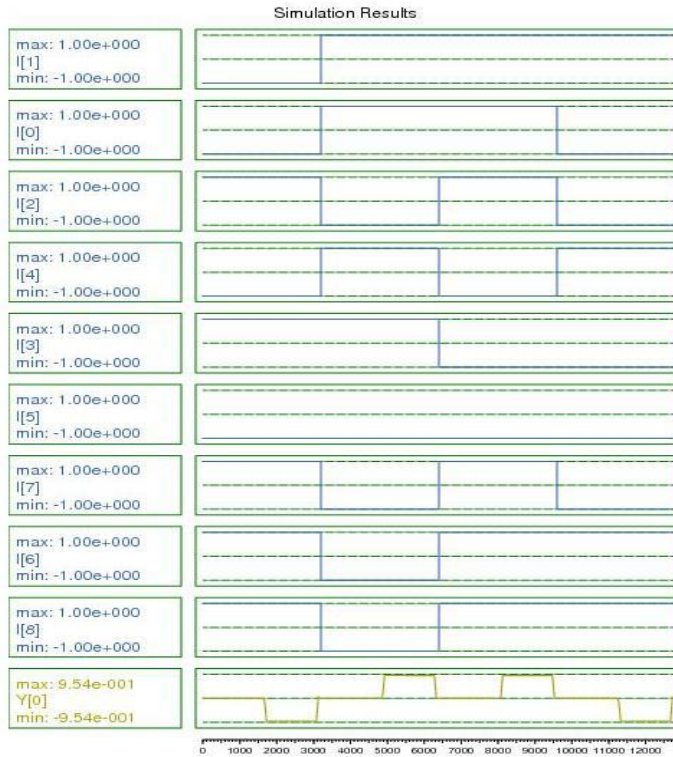


**Figure 5.** QCA layout of Majority gate based Median finding architecture.

#### 4. Result Analysis

The result of the median filter layout simulation is displayed in Figure 6. From the simulation result, it can be verified that there is a delay of 0.5 clocks. Figure 7 shows the QCA layout of the 4-bit numbers median finding architecture. The cell complexity, area and delay analysis of the proposed architecture are shown in below Table 1.

In this table for 1-bit architecture only 4 numbers of majority gates needed, with a delay of 0.5clk. For designing 2-bit architecture 16 numbers of majority gates needed with a delay of 0.5 clk. The 4-bit architecture needed 64 numbers of majority gates with a delay of 0.5 clk. Similarly  $n$ -bit architecture have  $4 \times 2^n$  number of majority gates with a constant delay of 0.5 clk. From the result of Table 1, it can be concluded that proposed architecture has achieved greater performance in speed, compared to other parameters when the size of the architectures are increasing, because the delay is constant irrespective of the size.



**Figure 6.** Simulation result of a majority output of a single column.

**Table 1.** Result analysis of the median finding QCA layouts.

Median filter	Number of Majority gates	Number of Cells	Total Area	Delay
1-bit	04	21	0.05 $\mu\text{m}^2$	0.5 clk
2-bit	16	84	0.2 $\mu\text{m}^2$	0.5 clk
4-bit	64	336	0.8 $\mu\text{m}^2$	0.5clk
8-bit	1024	5376	12.80 $\mu\text{m}^2$	0.5 clk

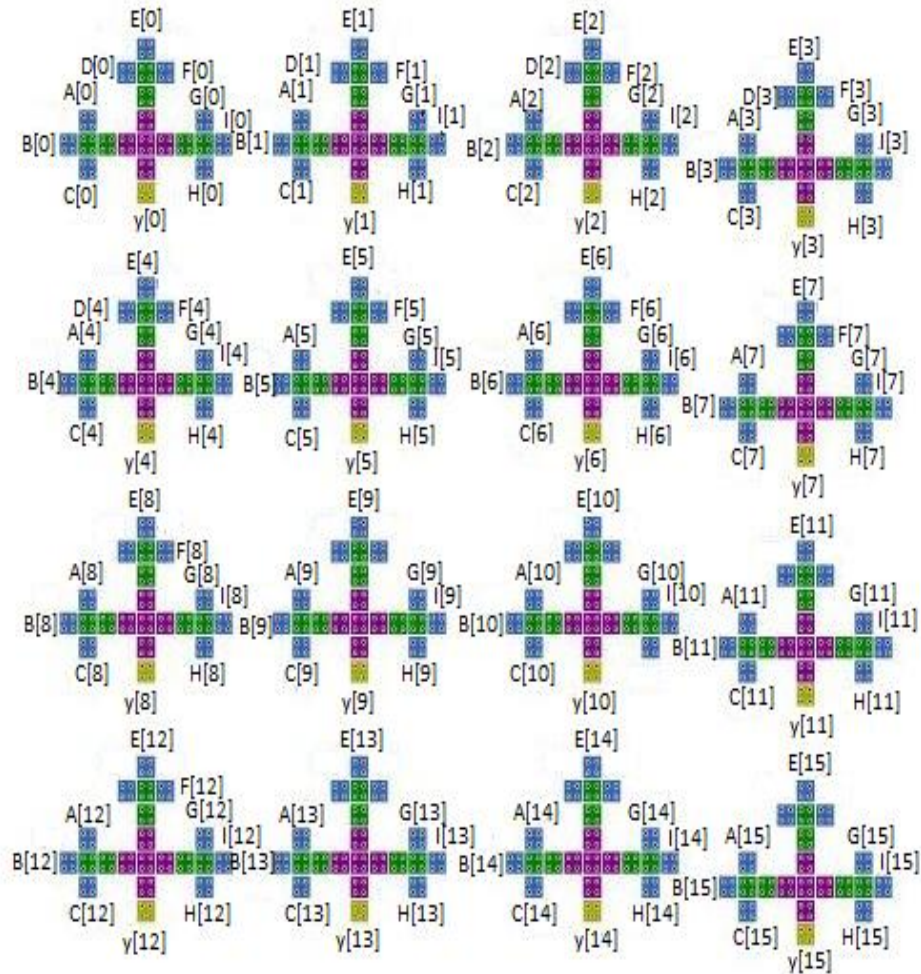


Figure 7. QCA layout of 4-bit numbers median finding architecture.

### 5. Conclusion

In this chapter, a new median filter is designed using majority logic-based technology. One hot encoding technique is used in the proposed architecture, which consumes low power compared to a binary encoding technique. The proposed  $n$ -bit median filter layout requires  $4 \times 2n$  numbers of majority gates. This filter can be used in image processing and any median finding related applications.

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