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A STUDY ON FERROELECTRIC FIELD EFFECT TRANSISTORS (FE-FET) BASED FERROELECTRIC RANDOM ACCESS MEMORY (FE-RAM)

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Abstract

With existing memory solutions, many barriers are rising among moore's law. The present existing embedded NVM (eNVM) market is influenced by embedded NOR-type flash which works fine and will be in market for many years but as it is scaled to more advance process node it increases in cost. While DRAM which is based on 1T-1C memory cell, has problems while scaling also due to its stacked capacitor there is increase in cost. Ferroelectric Field Effect Transistor (FeFET) based FeRAMs are widely used in smart cards and Integrated Circuits (IC) tags because of their numerous features like nonvolatile property, operational speed is more as compared to Dynamic RAMs (DRAMs) and less power consumption. This paper presents the study of FeFETs and FeFET based FeRAMs.

1. Introduction

Ferroelectric Field Effect Transistors (FeFET) have numerous advantages that include low power dissipation, high density integration, good scalability and non-destructive readout operation [1]. Over the past decades, a range of

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FeFETs have been investigated [2-9]. FeFETs are used for making ferroelectric memories. The ferroelectric memories were first introduced by bell laboratories in 1995. While the first Silicon based FeFET was introduced in 1974 [16]. A film of Bi4Ti3O12 was deposited on Silicon Si (100) substrate which acts as gate insulator and hysteresis loop was observed. If the electrical properties at the interface of semiconductor and ferroelectric are good, the device operates as *n*-channel *E*-type FET. With use of proper and optimized process and materials, it is possible to re-write data more than 1012 times which started the era of FeRAMs [17]. FET type FeRAM is shown in figure 1. The typical cell structure of FET type FeRAM is 1T-Type. Another type for FeRAM is capacitive type FeRAM which again uses 1C-1T type structure similar to DRAM. FeRAM finds most applications in smart cards and Integrated Circuit tags.

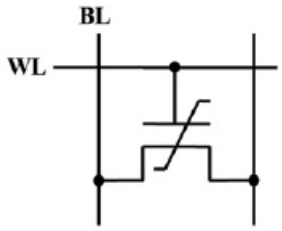

Figure 1. 1T type FET based FeRAM.

As compared to DRAM which uses 1C-1T type as shown in Figure 2, FeFET based FeRAM is composed of single FeFET so cell size can be scaled using proportionality rule. The advantage is that the data which is stored can be read out non-destructively using drain current of FeFET.

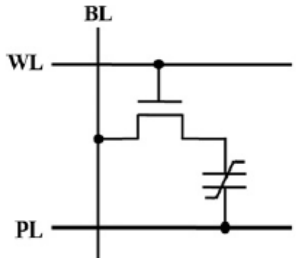

Figure 2. Cell structure of DRAM 1C-1T type.

II. Working of Ferro Electric Field Effect Transistor

Working of FeFET can be considered as a logic transistor which can maintain tits logic state even after the removal of power. The conventional logic gate dielectric is replaced by ferroelectric material in FeFET.in FeFET, within gate dielectric itself a permanent dipole is formed. Splitting the VTH(Th reshold Voltage) of ferroelectric transistor in two stable states. As like flash memory cell, binary states can be stored in these FETs. Figure 3-5 shows working of n type FeFET, when ferroelectric polarization points downward channel is inverted by electrons making FeFET into "on" state permanently. If ferroelectric polarization points upward, accumulation is created permanently and FeFET goes to "off" state. FeFET provides faster switching with low power consumption.

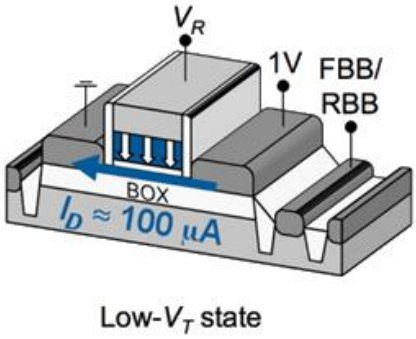

Figure 3. "On" state of FET.

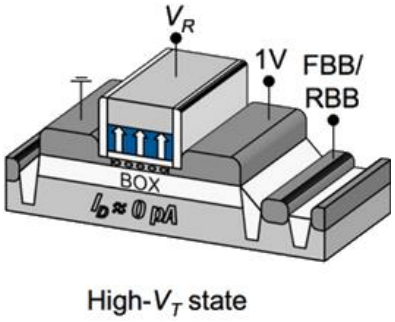

Figure 4. "Off" state of FET.

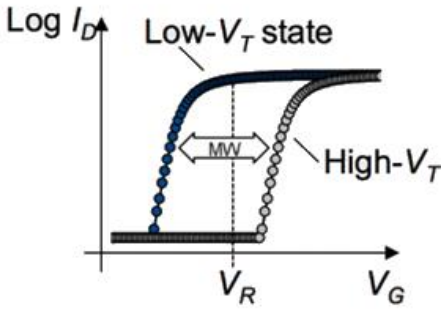

Figure 5. Ferroelectric Polarization.

III. Progress of Ferroelectric Field Effect Transistors

The material combination for the gate stock of the MFIS which was discovered in 2002 Pt/SrBi2Ta2O9/(HfO2)x(Al2O3)1−x/Si.Here after, and Hf-Al-O and SBT are (HfO2)x(Al2O3)1−x and SrBi2Ta2O9, respectively. The cross section of the schematic is shown in Figure 6.

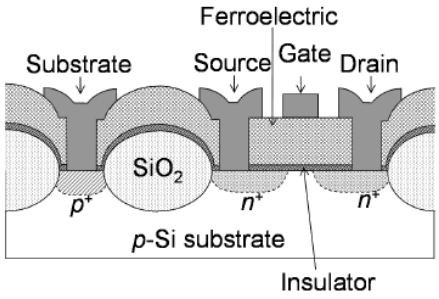

Figure 6. Cross sectional view of FeFET.

The n-channel MFIS FET for $x = 0.75$ characteristic for drain current Id and gate voltage Vg is given in Figure 7 [12].

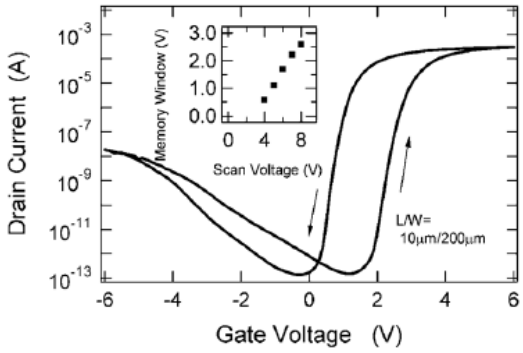

Figure 7. Curves for drain current and gate voltage of an n-channel Pt/SBT/Hf-Al-O/Si FeFET at Vg = ±6.0 V.

The curves are made at different values of Vg such as at Vg = ±4.0V, ±5.0V, ±6.0V, ±7.0V and ±8.0 V. The inset is made.

The gate voltage Vg is applied from −6.0 V to +6.0 V to obtain a hysteresis loop with 1.6V of wide memory window and a large drain current Id. 107 ratio of Id,on/Id, off with gate voltage vg at 1.7V because of the ferroelectricity. The increase in the drain current Id at negative values of the gate voltage Vg which is shown in figure 7 is because of the current between the n+ drain and p-type substrate and not due to the leakage current at gate. The increase in the drain current Id is correlated to the drain and gate length which is overlapped. There is decrease in the increase of drain current at the negative gate voltage when the length of the drain and gate is decreased. Therefore, the current which is increased at the negative gate voltage is GIDL meaning Gate Induced Leakage Current in between the inversion layer p and the drain bulk n+. [12]. Figure 8 shows characteristics of Id data retention in the MFIS FET [10-15].

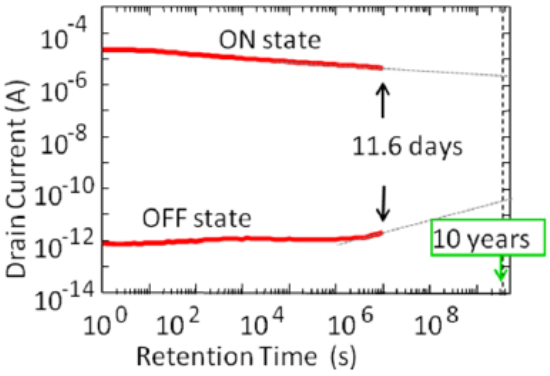

Figure 8. Characteristics of drain current retention of a Pt/SBT/Hf-Al-O/Si FeFET.

The gate voltage Vg is kept at Vkeep of 1.7v (bias gate voltage) for the measurement of drain current Id and gate voltage Vg of +6.0V is applied for the polarization of ferroelectric SBT The gate voltage Vg is at the same bias gate voltage for the measurement of Id, off. When Vg is at -6.0V applied, Vkeep is at 1.7V. The characteristic of Id, on and Id, off were measured for 12 days. Their ratio was 107 showing the plot between memory window and amplitude of applied gate voltage Vg. There is no saturation in the polarization of ferroelectric at 8.0 V scan voltage. For long retention of FeFETs, saturated polarization is not required. Long retention means that the working of non volatile FETs can be done when depolarization is present in the gate stack of MFIS.

IV. Necessary Properties of Ferroelectric RAM

A ferroelectric material exhibits a polarization when external electric field is not present and the direction of the spontaneous polarization can be reversed by an external electric field. In the state of ferroelectric, the positive charge centre in a unit-cell in the crystal which dp not coincide with the negative charge centre. A typical plot of polarization versus electric field (P-E) in a ferroelectric film is shown in figure 9. In which the coercive field EC is the reverse field necessary to bring the polarization to zero, and the remanent polarization Pr is the value of P at $E = 0$ in the case of the FET-type

FeRAM, since the ferroelectric film is used as the gate insulator of an FET, the large remanent polarization is not necessarily important, but the low reactivity of the ferroelectric film with the semiconductor substrate or with the insulating buffer layer is more important.

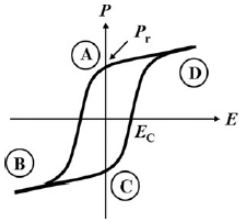

Figure 9. P-E hysteresis loop in ferroelectric film.

In the following, typical degradation mechanisms in the ferroelectric films are discussed. Polarization fatigue describes that the remnant polarization *Pr* becomes smaller when a ferroelectric film experiences a large number of polarization reversals. Variation of the hysteresis loop due to fatigue is shown schematically in Figure 10. Because of the decrease of *Pr*, the charge difference between logic "0" and "1" becomes smaller and this phenomenon can lead to a failure in the "read" operation. The physical origin of fatigue is not very clear, but the following factors will be related to the phenomenon: domain wall pinning by charged defects, inhibition of domain nucleation by injected charges, and voltage drop at the interfacial layer between the ferroelectric film and the electrode. The fatigue endurance in FeRAMs is known to be typically1012 switching cycles. Thus, it is difficult at present to use FeRAMs in such applications as a cache memory, in which data are continuously rewritten during "write/read" operations.

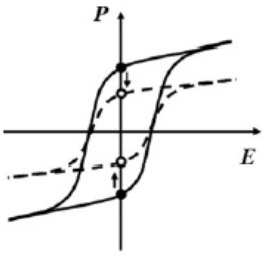

Figure 10. Fatigue in hysteresis loop.

When a ferroelectric film experiences a high DC voltage or repeated unipolar pulses for a long time, particularly at high temperature, its polarization is not fully reversed by application of a single voltage pulse with the opposite polarity. Imprint leads to a P-E hysteresis loop shift on the axis of electric field, as well as to a loss of *Pr*, which is shown in Figure 11.

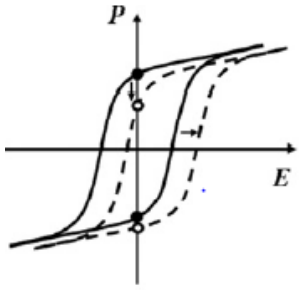

Figure 11. Imprint in hysteresis loop.

Hence, imprint can result in either "read" or "write" failure of the memory cell. Retention loss describes a decrease of Pr during an absence period of the external voltage, as shown in Figure 12.

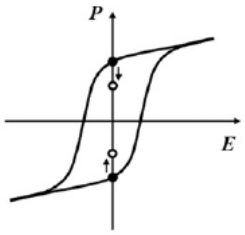

Figure 12. Retention loss in hysteresis loop.

Conclusion

A numerous advantages of FeRAMs which include lesser power dissipation, more integrity, less consumption of power and nondestructive read out operation of FeRAM over the traditional DRAMs and flash memories. A study has been carried out for Ferroelectric Field Effect Transistor FeFET) and FeFET based Ferroelectric RAMs. Different design considerations have been discussed. The main application of FeRAM are IC

tags and Smart cards. The research is being carried out also on organic ferroelectric films that can be used as gate insulators.

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