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STUDY AND PERFORMANCE ANALYSIS OF REDUCED SWITCH COUNT ASYMMETRIC 31-LEVEL INVERTER

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Abstract

Multilevel inverters, which require far minimum dc sources and switches to produce minimal switching, high power and lower harmonic distortion for moderate operating voltage, have been the focus of academics and enterprise. Even so, there are certain drawbacks to multilevel inverters, such as the employment of numerous electronic components, EMI, bulkiness, driver circuit complexity, long reverse recovery periods and voltage balance concerns. This article introduces a unique asymmetrical multi-level inverter (MLI) that uses lesser drivers and switches than standard implementations. The recommended MLI has a simple architecture and is straightforward to extend for a variety of output levels. The suggested MLI system uses four dc sources and twelve switches to produce a 31-level output including an accurate and high-quality near sinusoidal waveform, resulting in a large decrease in driver circuit complexity, volume and price. The proposed architecture includes reduced ON state semiconductor switching devices, which is a novel feature. The MLI's output is evaluated using the total harmonic distortion (THD) factor. To reduce THD, sine pulse width modulation approach has been implemented. The comparative analyses along with MATLAB/Simulink results are presented.

1. Introduction

In the domains of electric energy generation, transmission, distribution, and usage, inverter has become a vital technology. Inverters are essential to

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achieving this goal in a number of vital areas. Inverters are divided into two types based on the output waveform: two-level inverters and multilevel inverters. The main issue concerning two-level inverters is that they necessitate devices with large power ratings, which are not always available, and hence several devices must be coupled in series or parallel chains to acquire the requisite voltage/current competence. Some other issue with these inverters is their low output power quality and the need for filtration. As an alternative, the multilevel inverter construction is presented for such power levels.

Cascade multilevel inverters are recommended in classic configurations because they require fewer components than other multilevel inverters and are easier to adapt to many voltage levels. Power may be easily amplified in cascaded multilayer inverters by using a succession of power conversion cells. Every cell has one H-bridge and the multilayer inverter's output voltage is the total of all the voltages created by all the cells. To manage the amount of power given to the load without wasting power, several pulse width modulation techniques have been developed for multilevel inverters. Pulse width modulation technology is separated into level shifted and phase shifted PWM on the carrier signal layout. This study focuses on the use of appropriate modulation techniques to reduce overall harmonics distortion of output voltage and build a 31-level inverter with the fewest possible DC voltage sources, switching devices and driver circuits. MLIs are commonly utilized in energy and power systems, as well as regenerative conveyors in manufacturing and transportation. Multilevel inverters have evolved from a cutting-edge technology to a well-established and appealing medium-voltage high-power solution. The constant advancement of technology, as well as the growth of industrial applications, will present new difficulties and opportunities for multilayer inverter improvement.

2. Literature Review

The simplest configurations for a cascade multilayer inverter were described [1-3]. All of the employed dc voltage sources have the same amplitude, which is known as symmetric setup [1]. However, the amplitude of dc sources is unequal, which is referred to as an asymmetric arrangement [2, 3]. The number of produced levels is more in an asymmetric structure than in

a symmetric design. Novel basic structures have been created that have fewer components and can only produce positive output voltage waveforms [4, 5]. As a result, generating negative voltage levels necessitates the use of an H-bridge. The current channel's voltage stress on H-bridge switches and the number of on-state switches are both high, resulting in significant power losses. Another enhanced cascading multilevel inverter structure presented that can be employed as both symmetric and asymmetric [6]. The suggested multilevel inverter also has the advantage of increasing the number of output voltage levels while reducing the number of power electronic components. New fundamental unit structures that can yield greater voltage levels have been reported [7-9].

The main disadvantages of these systems are higher voltage stress on H-bridge switches and the use of multiple bidirectional switches. [10, 11] has detailed other cascaded structures based on serial connecting produced H-bridges. [12] proposes a new switching capacitor-based cascade multilayer inverter. The most notable benefit of this setup is the presence of a common ground for all capacitors and the dc source. Because this architecture has a large number of on-state switches, it is inefficient. Without the need of an H-bridge, this topology may generate all positive and negative levels. [13] describes the basic structure of a cascaded multilevel inverter that can generate both positive and negative output levels without using an H-bridge. In this architecture, the current path has a maximum of three on-state switches. By merging many basic units and employing an H-bridge as the output, numerous improved cascade multilevel inverters have been developed [14]. This design proposes a superior multilevel inverter that can generate positive and negative levels even without usage of an H-bridge. In the suggested topology for the same number of levels, the ratio of generated levels to the number of sources and switches is high when compared to earlier designs. For all RL load values, this inverter is appropriate.

3. Proposed Configuration of 31-level Asymmetrical MLI

Figure 1 shows the proposed 31-level inverter, which contains four dc voltage sources (V_1, V_2, V_3, V_4), 12 power switches consisting of 12 unidirectional switches $(S_1, S_2, S_3, S_4, S_5, S_6, S_1', S_2', S_3', S_4', S_5', S_6')$. The produced

levels from switching states of the 31-level inverter are: 0, 25, 50, 75, 100, 125, 150, 175, 200, 225, 250, 275, 300, 325, 350, 375 Volts. The resultant voltage may be calculated using close loop analysis in the proposed arrangement, as illustrated in Figure 1.

The amplitude of dc voltage sources influences the number of derived voltage steps. The amplitude of dc voltage sources is often chosen to generate the greatest number of levels. To achieve this, the 31-level inverter's dc sources are set to $V_1 = V_{dc}$, $V_2 = 2V_{dc}$, $V_3 = 4V_{dc}$, $V_4 = 8V_{dc}(V_{dc} = 25V)$. The proposed structure can thus generate 31 voltage levels (15 +ve, 15-ve, and 0) at the output voltage waveform.

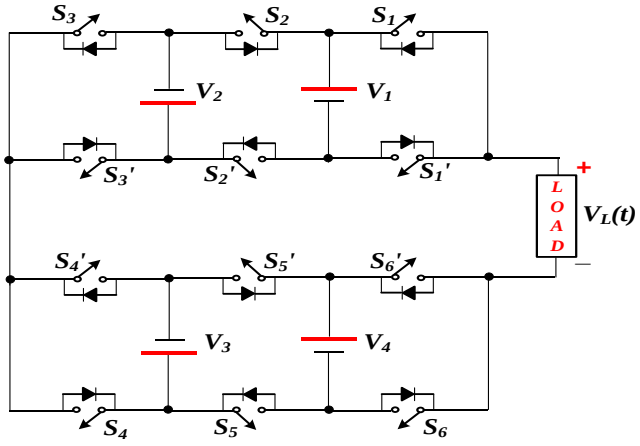

Figure 1. MLI based on a 31-level asymmetric source.

The most important factor impacting inverter losses, pricing, and capacity is voltage stress on switches. Table I shows the voltage stress on the planned 31-level inverter's switches.

Table I. Voltage stress on the switches in the developed system.

Switch	Stress on the voltage	Voltage Stress (Normalized)	Switch	Stress on the voltage	Voltage Stress (Normalized)
S1	V_{dc}	V_{dc}/15Vdc= 6.66%	S1'	V_{dc}	V_{dc}/15Vdc= 6.66%

S2	3Vdc	3Vdc/15Vdc= 20%	S2'	$3V_{dc}$	3Vdc/15Vdc= 20%
S3	2Vdc	2Vdc/15Vdc= 13.33%	S3'	2Vdc	2Vdc/15Vdc= 13.33%
S4	4Vdc	4Vdc/15Vdc= 26.66%	S4'	4Vdc	4Vdc/15Vdc= 26.66%
S5	12Vdc	12Vdc/15Vdc= 80%	S5'	12Vdc	12Vdc/15Vdc= 80%
S6	8Vdc	8Vdc/15Vdc= 53.33%	S6'	8Vdc	8Vdc/15Vdc= 53.33%

According to table I, the real value and normalized voltage stress on switches S1, S1' are V_{dc} and 6.66 %, respectively. On switches S2, S2', the true value and normalized voltage stress are 3Vdc and 20%, respectively. Furthermore, on switches S3, S3', the true value and normalized voltage stress are 2Vdc and 13.33% respectively. On the switches S4, S4' and S6, S6', the true value and normalized voltage stress are 4Vdc and 26.66%, 8Vdc and 53.33% respectively. The highest voltage stress on the switches S5, S5' is 12Vdc with an 80% normalized value. The switches are under less voltage stress than the output voltage's maximum value.

4. Simulation Study

A simulation study is conducted using the MATLAB software application to validate the functionality of the suggested asymmetrical MLI setup as shown in Figure 1. A thirty-one level inverter with two cells and four asymmetric sources with $V_1 = 25V$, $V_2 = 50V$, $V_3 = 100V$ and $V_4 = 200V$ are used to model the suggested MLI design. At the output terminals, an RL load with $R = 40$ and $L = 4.25$ mH is evaluated.

As carriers, phase oriented triangular pulses with a frequency of 2 kHz are utilized, with a sinusoidal reference with a frequency of 50 Hz. The 'universal control scheme,' which is implemented in [7], is used to modulate the topology. Figure 2 and figure 3 shows the load voltage $(V_L(t))$ and

harmonic profile respectively. Figure 4 and figure 5 show the load current waveform and harmonic spectral response, respectively.

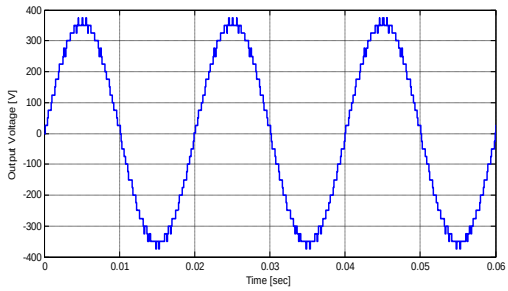

Figure 2. Load voltage $(V_L(t))$ waveform for 31-level cascaded inverter.

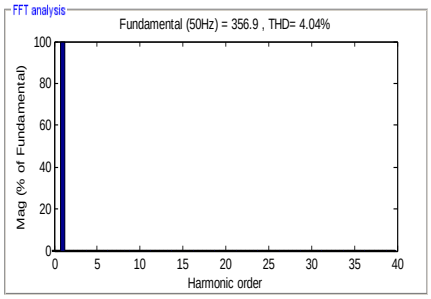

Figure 3. Harmonic profile of load voltage.

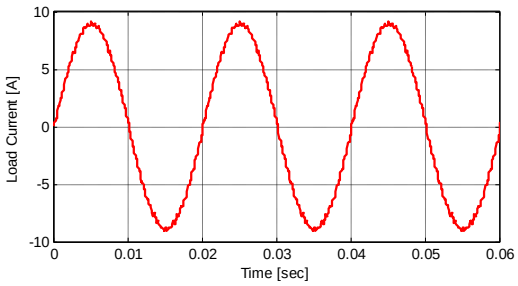

Figure 4. Asymmetrical MLI load current waveform with RL load ($R = 40\ \Omega$ and $L = 4.25$ mH).

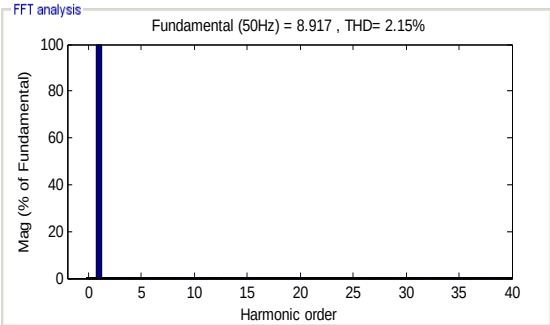

Figure 5. Harmonic spectrum of load current.

5. Conclusion

This research proposes a 31 level converter topology based on asymmetrical sources. The suggested multilevel inverter uses the fewest dc voltage sources, IGBTs and switches possible. It also reduces the proposed system's cost, weight, losses and bulk. THD is then reduced to 4.04%, as per IEEE standard 519, without the use of filters. In addition, a multicarrier PWM approach is used to optimize the shifting frequencies of multiple power switches under voltage strains. Simulation findings on a suggested 31level inverter are used to confirm the established theoretical characteristics. The recommended structure is utilized in high power applications.

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