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APPLICATIONS OF PULSED LATCHES AND BIDIRECTIONAL PULSED LATCHES

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Abstract

In recent years area and power consumption is given utmost importance to the digital designs. Most of the designs include flip-flops in their architecture. Some of the applications of flip-flops include storage register, storage register (Bidirectional), Ring and Johnson counter etc. There are many methods to reduce area of circuit; proposed method uses the replacement of conventional components with new and improved components. One of the components that can replace flip-flop is pulsed latch. Many studies have shown and proved that using pulsed latches reduce area and time consumption. Thus making the circuit area efficient and time efficient. In this paper, the design of bidirectional storage register using is implemented with pulsed latches and also low area architecture for Ring counter and LFSR using pulsed latches has been proposed. This proposed design is developed with Xilinx ISE 14.7 software using Verilog language.

1. Introduction

Shift registers are circuits (digital) are constructed using flip-flops. Flip-flops are connected serially and form the storage register circuit which is able to shift the data either towards left or right depending on indication by direction signal. Similarly bidirectional storage registers are constructed using flip-flops (master-slave fashion) and 2 to 1 multiplexers which are able to shift the data towards both the directions i.e. towards right and towards left, depending on the control signal direction. Traditional circuit for bidirectional storage register is shown in Figure 1.

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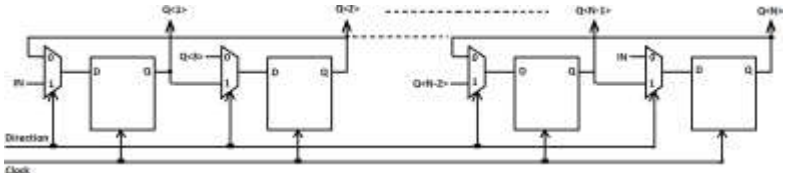

Figure 1. Conventional Nbit Bidirectional storage register using N, 2:1 MUX and N, Master-Slave flip-flops [12].

Figure 2. Shows the circuit of bi-directional storage register constructed using master-slave flip-flops.

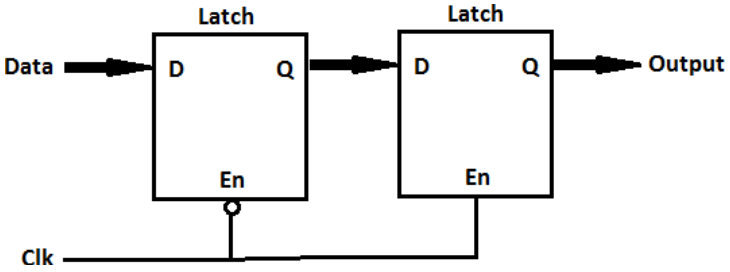

Figure 2. Master-Slave flip-flop arrangement [12].

In [1], a 256-bit low area architecture of bi-directional storage register is implemented using 65nm CMOS technology. In this design, pulsed latches and non overlapped clock signals are used to replace the traditional master slave flip flops and two 2-1 multiplexers hence 39% area saving is achieved. Area and power saving is estimated in the design [2] by using pulsed latches in place of flip flops. To solve timing problem group of latches and combination of non overlapping pulsed clock signals for the limited storage time period are used to save the power as estimated in [3]. Designing systems using pulsed latches has shown lot of dynamic power saving [4] in nano-meter scale design. The novel way of designing ring counter [5] using pulsed latches improves the speed of operation of counter by decreasing power delay product. The significant reduction in clock signal power is achieved by replacing pulsed latches in clock signal path in place of conventional flip flop reported in [6]. The power consumption of pulsed latches is lesser than an edge triggered flip flop and they can be efficiently used in different circuit design methodologies as reported in [7]. The area and power efficient heuristic algorithm is implemented considering pulsed latches using 45nm process technology in [8]. The effective way of pulse width integrity is

obtained in [9] by inserting framework of pulsed latches by reducing negative slacks with marginal interconnection lines. The LFSR key stream generator [10] which uses pulsed latches is used in encryption of audio data with reduced system complexity. Hence, the proposed work discuses here is an efficient way of designing applications like ring counter, bidirectional shift register and LFSR used stream generator using pulsed latches.

2. Proposed Architecture

Pulsed latches have shown an efficient way of implementation of sequential elements which replaces the flip-flops in various designs. Pulsed latches being special latches that are run by short pulses which are created from a traditional clock signal using a pulser circuit as given in Figure 3. Reduced power and time over heads are attained using pulsed latches than the design with flip-flops. Pulsed latches have an advantage of lower timing because one latch comes in between the input and the output.

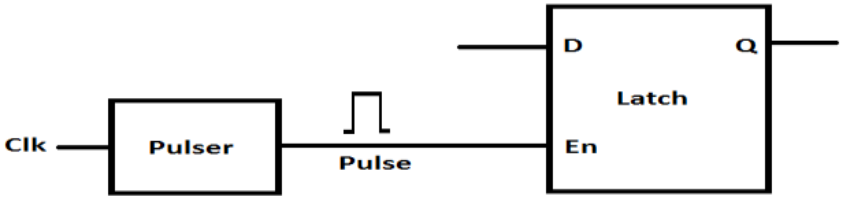

Figure 3. Architecture of simple Pulsed Latch with Pulser circuit.

One of the disadvantage with pulsed latch while using in bidirectional storage register circuit leads to be race round condition. This can be avoided by using temporary extra latches. Below figure 4 shows the bidirectional latch used in bidirectional shift register circuit. DR is input data to be shifted towards right, which will be present at QR after a clock pulse CLK_R. Similarly DL is input data to be shifted towards left, which will be present at QL after a clock pulse CLK_L.

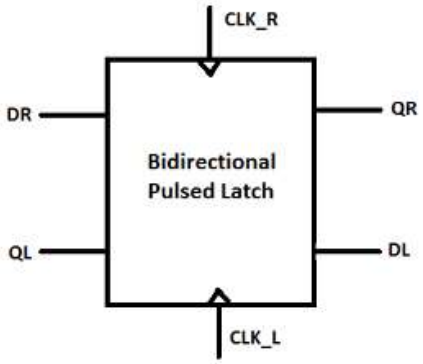

Figure 4. Architecture of bidirectional pulsed latch.

2.1 Proposed Architecture for Bidirectional storage Register

The figure 5 shows the architecture of bidirectional storage register with bi-directional pulsed latches (BD-PLs). This architecture consists of two main components, namely BD-PLs and circuit of bi-directional delayed pulsed clock generator. The grayed BD-PLs are temporary BD-PLs used to avoid race round condition in any circuit. The below architecture shows 4-bit bidirectional storage register implementation. The working of the circuit is as follows: if 'Right' signal is made high, the clock pulses generated are CLK_pulse_R<T> to CLK_pulse_R<4> and shifting the data towards right. Similarly when 'Right' signal is made low the clock pulses generated are CLK_pulse_L<T> to CLK_pulse_L<4> and shifting the data towards left.

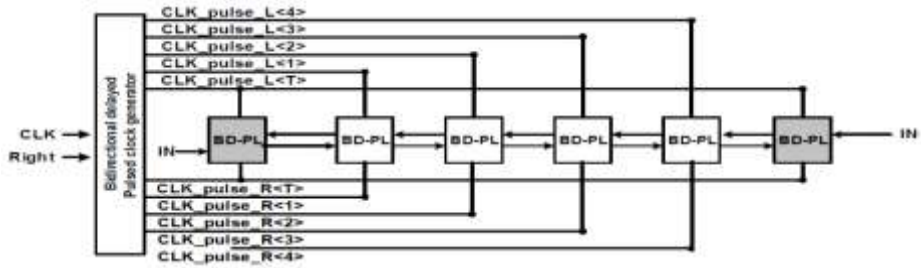

Figure 5. Proposed architecture for 4-bit bidirectional storage register using BD-PLs.

2.2 Proposed Architecture of 8-bit Ring Counter

The Ring counter which is of 8-bit can be implemented using 8D latches.

The D-latches are connected in series such that the output of last latch is given as feedback input fed to first *D* latch. The Q1 output of the pulsed latch 1 is connected to input of the pulsed latch 2 etc. The pulse generator circuit generates clock pulses. The pulse generated by clk_pulse_1 is given as input to *D* latch 1, clk_pulse_2 is given as input to *D* latch 2 and so on. The 8-bit ring counter implementation require 8 clock pulses. The delayed clock pulses generated are shown in Figure 6.

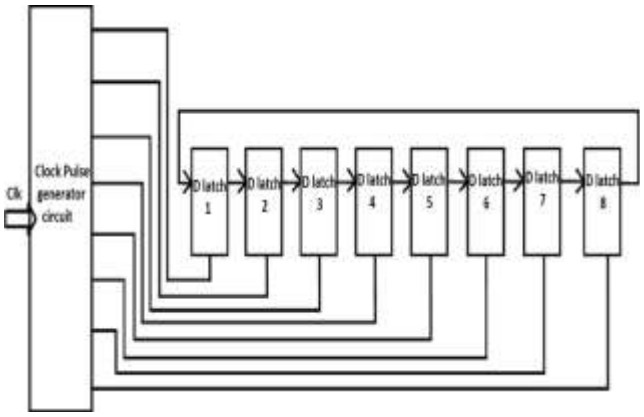

Figure 6. Proposed architecture of Ring Counter using Pulsed latches.

Clock pulse generator also derive other clock signals by taking reference clock signal and dividing it namely called as delayed clock pulses. Depending on the application the number of clock pulses will be generated. In the proposed paper, implementation of 8-bit Ring counter is illustrated. This implementation require 8 clock pulses. Generation of 8 clock pulses with minimum clock period of TCLK_MIN=TCP+8XTDELAY had been considered.

2.3 Proposed Architecture of ASG using LFSRs

To design area efficient and time efficient Alternating step generator, LFSRs used in ASG circuit can *b* designed using pulsed latches instead of *D* flip-flops. Below figure, Figure 7 shows the internal circuit of LFSR designed using pulsed latches or *D* latches, sometimes also called as transparent latches due to their operation. The circuit consists of 5D latches, thus 5 clock pulses are required to enable the latches. The clock pulses with shorter clock period can be generated using clock pulse generator circuit.

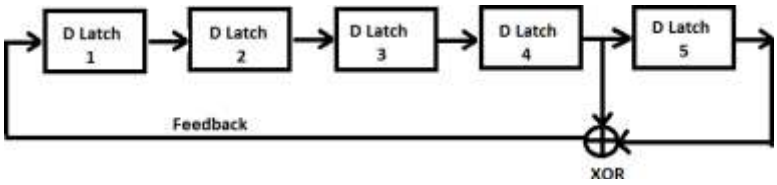

Figure 7. 5-bit LFSR using pulsed latches.

3. Implementation Results

The proposed applications such as ring counter, bidirectional shift register and LFSR are coded in verilog language and functional verification results are obtained in the form of simulation results as shown in Figure 8 to Figure 10.

Figure 8. Simulation results of bidirectional shift register using BD-PLs.

Figure 9. Simulation results of 8-bit ring counter using BD-PLs.

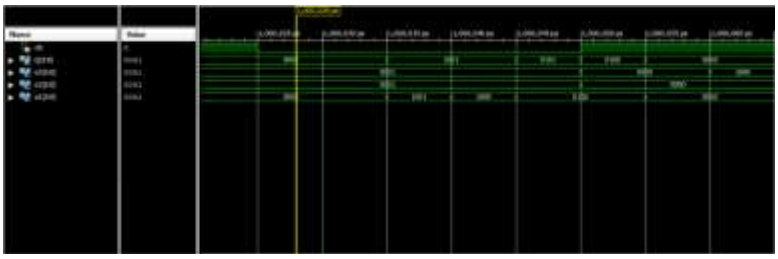

Figure 10. Simulation results LFSR using BD-PLs.

Further, all the application designs are implemented on Sptran-3 FPGA board. The area and delay analysis of all the designs are reported in Table I, and II.

Table I. Delay comparison of Bidirectional shift register, Ring counter and LFSR using PLs.

Clock Domains	Conventional BDSR	BDSR using BD-PLs	Conventional Ring Counter	Ring Counter using PLs	Conventional LFSR	LFSR using PLs
Total Real time	22 Secs	18 Secs	58 Secs	48 Secs	28 Secs	21 Secs
Total CPU time	22.80 Secs	17.88 secs	50 Secs	44 Secs	27 Secs	20.93 Secs

Table II. Area comparison of Bidirectional shift register, Ring counter using PLs.

Device Utilization	Conventional BDSR	BDSR using BD-PLs	Conventional Ring Counter	Ring Counter using PLs
BELS	5	1	8	2
Flipflops	8	0	8	0
GND	1	1	1	1
IO Buffers	16	16	1	1
OBUF	14	16	8	8

4. Conclusions

Proposed area efficient bi-directional pulsed-latches can be implemented with pulsed latches replacing master slave flip-flops and 2-to-1 MUXs. The issues need to addressed with pulsed latches are avoid the situations of race round condition. The problem can be mitigated with use of non-overlap delayed pulsed clock signals in place of single pulsed clock signal. Ring counters are one of the widely used digital circuits which can be used in many desired applications like frequency divider and counting the data etc. The Ring counter implantation in the proposed paper shows requirement of smaller area with pulsed latches. The delay analysis indicates that an improved speed of operation of proposed applications using pulsed latches compared to conventional ones. So, the pulsed latches which consume less time while in operation will replace the existing flip-flops in near future.

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