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ADIABATIC ADDER: MODELING, DESIGN AND SIMULATION

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Abstract

The main goal of this paper is to present new low power technology for portable electronics and SOC industry. The main focus of our research is the power dissipation, area and speed. These parameters are showing an ever-increasing growth with scaling down of the technologies. The full adder is the most important component of any digital circuits and systems. To minimize the power dissipation, several approaches are there and all the schemes have their own limitations. Here in this work we have presented a novel scheme known as energy recovery or adiabatic logic. We have implemented adder using two different types of energy recovery technologies and compare the results with CMOS technology based adder. The results show a great percent of power saving in case of energy recovery or adiabatic logic. The simulation is done using Tanner EDA tool.

1. Introduction

Now a day's power dissipation is more important problem in portable and high performance electronic devices. This power dissipation causes the reliability problems. So energy efficiency has become the major concern in the portable equipments to get much better performance with minimum power dissipation. To overcome the power dissipation extra circuitry is necessary to incorporate in the devices and to protect the device from thermal breakdown.

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This also results in increase of total area of the system. In order to overcome these problems the power dissipation of the circuit is to be reduced by adopting various low power technologies. [2], [3]. The main sources of power dissipation are static power consumption, dynamic power consumption and short circuit power consumption. Majority of power is dissipated in pull up network of conventional CMOS network and remaining power is stored on node capacitor. This stored charge is wasted in ground. But, it can be recycled back and reused as power clock again. It is mention in thermodynamic process which is a reversible logic. The adiabatic logic is worked on this thermodynamic principle and it can recover the partial or whole power from the load. In this paper we have presented adiabatic logic based adders and estimated the power dissipation and delay parameters of these adder circuits.

2. Adiabatic Logic

The word adiabatic originates from a Greek word that is utilized to describe thermodynamic processes that exchange no energy with the environment and therefore, no energy loss in the form of dissipated heat. Such ideal process cannot be achieved because of the presence of dissipative elements like resistances in a circuit. However, we can achieve very low energy dissipation by decelerating the speed of operation and only switching transistors under certain conditions. The energies stored in the circuit capacitances are recycled instead, of being lost as heat. The adiabatic logic is also known as energy recovery logic [5]. Unlike the conventional CMOS circuits, in adiabatic circuits energy is recycled. Since the charge has to be discharged to power supply, the power supply in adiabatic circuits is a time varying one called the power clock. It has been noticed that among various waveforms for charging or discharging the load capacitor, a ramp is more efficient and as such trapezoidal power clocks have been used efficiently in many adiabatic circuits.

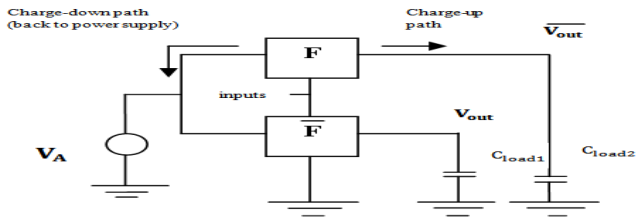

Figure 1. Adiabatic charging process.

In contrast to CMOS logic, adiabatic Logic doesn't suddenly switch from 0 to V_{dd} and vice versa, but a voltage ramp is used to charge and recover the energy from the output of the circuit. Let us take, R is the resistance offered by the charging path, which is the combination of the on resistance of transistor in the charging path and the sheet resistance of the signal line. It is assumed that R to be constant for the power calculations. A voltage value is increased gradually as a ramp function from value 0 to 1, the voltage increment should be slow enough so that is able to follow signal $v(t)$ instantly.

We know charge and voltage equation as: $Q = CV_{dd}$ is taken from the voltage source, an energy quantum of $EV_{dd} = QV_{dd} = CV_{dd}^2$ is withdrawn from the voltage source. The energy stored on the capacitor at the voltage V_{dd} is equal to $Ec = 1/2\,CV_{dd}^2$. Ec is the dissipated energy. The difference between the delivered energy and the stored energy is dissipated in the PMOS switch. Now, if the input switches from 0 to 1, in steady-state condition on the output capacitance the NMOS channel is on, the PMOS off. Charge stored is then dissipated via the NMOS device to ground.The energy dissipation of a switching event in a static CMOS gate is given as $E_{Cmos} = \alpha\, 1/2\, CV_{dd}^2$.

In adiabatic logic changeover occurs without energy being either lost or gained from the system rather than heat or electronic charge is preserved. Thus an ideal adiabatic logic would operate without increase or decrease of electronic charge. In this technique during switching process this logic reduces the dissipation of power or energy and whereas it reuses the energy by recycling it from the load capacitance, so that the same energy can be used for next cycle of operation.

3. ECRL Adiabatic Logic

ECRL logic is that in which precharge and recovery phases are simultaneously worked and by this implementation, the power dissipation is minimize up to greater extent. This method does not use the diode and generates less energy dissipation. Compared to other methods of energy recovery, it uses least number of PMOSFETS. It uses only two PMOSFETS for precharge and recovery phases. Due to this cross coupled PMOSFETS, the output is stored and it also charge and discharge the load capacitor according to the transition of the constant power supply of power clock [8].

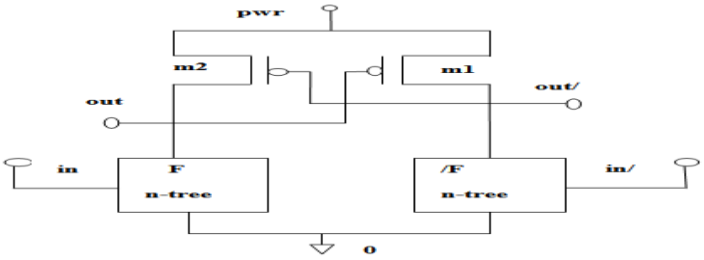

Figure 2. ECRL circuit diagram.

4. PFAL Adiabatic Logic

PFAL is partial or quasi energy recovery circuit and its core of all adiabatic circuit is made by adiabatic amplifier, a latch made up of two PMOSFETS M1-M2 and two NMOSFETS. Due to these MOS transistors, the logic level degradation on the outputs nodes can be avoided. Due to this process the out is connected to the ground and/out will be based on the changes of power clock. When the power clock reaches, out will become zero and or out will be turned to V_{dd} which will be act as an input for the next stage of the operation. Let us consider the power clock varies from V_{dd} to 0 then the energy will be recovered through the transistor M1. The functional blocks are connected in parallel with the PMOSFET of adiabatic amplifier.

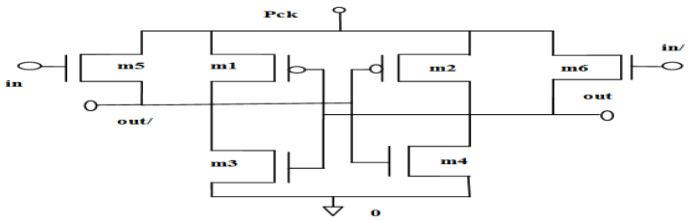

Figure 3. PFAL circuit diagram.

5. ECRL Adder

In ECRL technique, a power clock signal is differentiated into four phases: wait, evaluate, hold, and recover. During wait phase, an input signal is prepared by the previous logic gates. During evaluate phase, an input signals are kept stable and the gate outputs are calculated based on the stable signals. During hold phase, a supply voltage is kept constant to V_{dd} and the input signal is minimized. During recover phase, a clocked V_{dd} becomes lower and the energy from the output nodes is recycled during the discharging process.

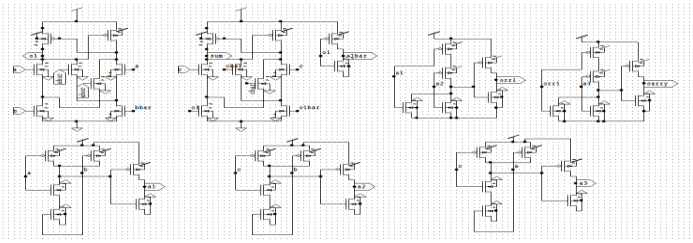

Figure 4. ECRL adder circuit diagram.

6. PFAL Adder

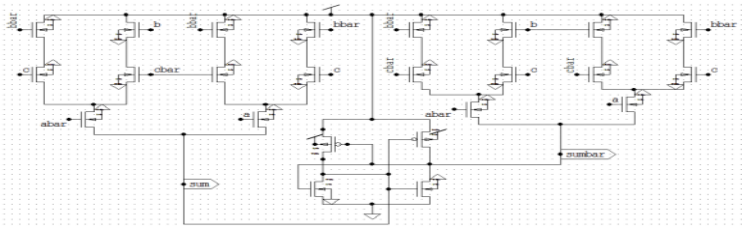

Figure 5. PFAL Adder Sum output circuit diagram.

PFAL is quasi adiabatic logic and it is same as the 2N-2P logic. The sum and carry equations are implemented on the bases of two NMOS and two PMOS transistors and it produces two outputs separately. PFAL logic which minimize the coupling effects and in construction, its logic is made up of two NMOSFETS and two PMOSFETS. A four phase power supply or power clock is used in PFAL, which performs the evaluate operation, hold operation, wait operation and recover operation. Here we have presented the PFAL based sum and carry circuits.

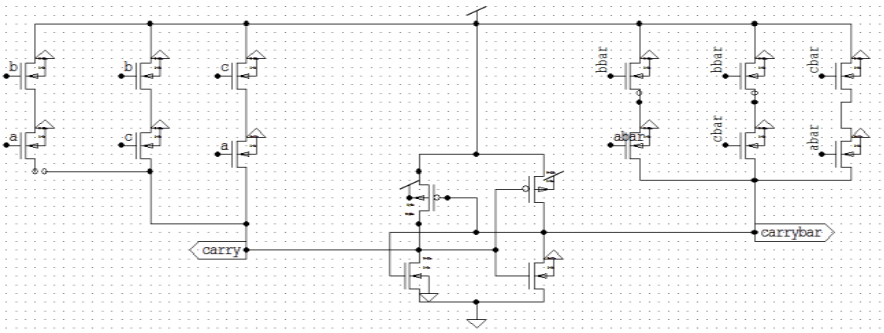

Figure 6. PFAL Adder carry output circuit diagram.

7. Simulation Results

The simulation waveforms and other simulation results for these two types of adders are shown.

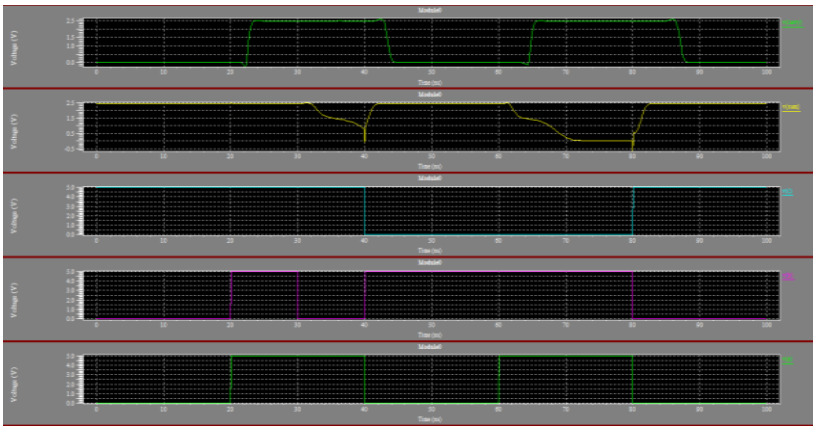

Figure 7. ECRL based adder output.

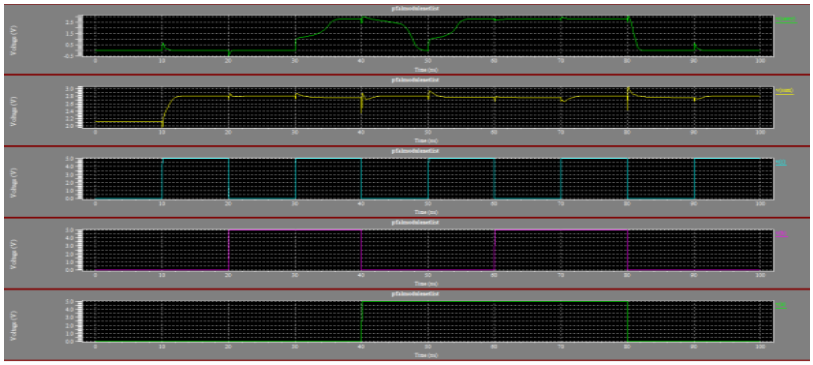

Figure 8. PFAL based adder output.

Table 1. Adder simulation results.

Parameter	ECRL	PFAL
Power supply	3.0v	3.0v
Average power	22.16 µw	11.08 µw
Transistor count	48	40

Table 2. Power dissipation measurement with frequency variations.

Frequency	ECRL	PFAL
20MHz	15.09 µw	13.01 µw
30MHz	10.15 µw	9.13 µw
40MHz	8.56 µw	6.23 µw

Table 3. Delay measurement with frequency variations.

Frequency	ECRL	PFAL
20MHz	10.02ns	3.21ns
30MHz	8.15ns	2.21ns
40MHz	6.25ns	1.13ns

8. Conclusion

The simulation results shows that positive feedback adiabatic logic (PFAL) based adders have better performance over efficient charge recovery logic(ECRL) based adders. The performance is better with respect to power dissipation, propagation delay and also chips area requirements. This type of adders that is PFAL adders can be used in portable, high speed and miniature electronic components. They are also good for ultra low power processors and embedded processors.

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